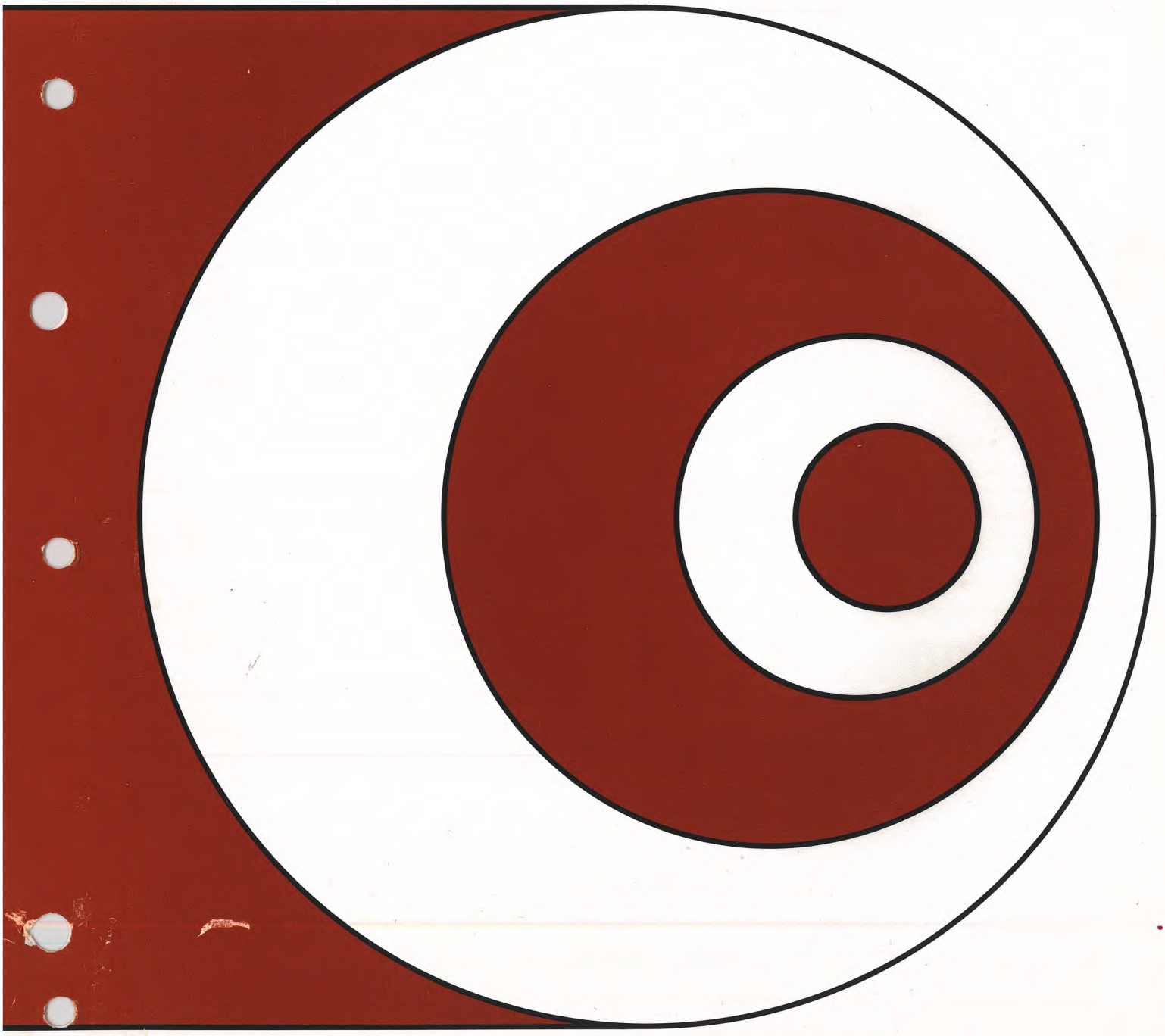
SIGNETICS TWIN

REAL TIME HARDWARE ANALYZER

SUPPLEMENT TO REFERENCE MANUAL



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SUPPLEMENT TO REFERENCE MANUAL

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1.0 REAL-TIME HARDWARE ANALYZER PRODUCT OVERVIEW

The Hardware Analyzer (HWA) provides the designer with a tool to monitor the user's system operation in real-time (through the TWICE cable) and detect faulty hardware or software logic. It also allows memory space to be mapped into segments, each of which may reside either internal to the TWIN (common memory) or within the user's prototype hardware (user memory).

1.1 PURPOSE

The basic TWIN hardware/software package is capable of supporting the early stages of prototype development in various "Debug" modes. It does not allow the user to monitor the system in real-time, because the slave unit is halted whenever its status is checked or displayed. This product is designed to support a prototype system development effort to the very end, where that system operates in a real-time environment.

1.2 TWIN SYSTEM WITH HWA

The HWA consists of an additional hardware/software package to the basic TWIN system of a single circuit board, and several supporting command overlays in the operating system (SDOS version 3.1 and up).

1.3 FEATURES

1. Real-time Trace of 256 bus transactions (address, data, and control).
2. 256 bytes of Shadow Memory (RAM) for utility programs.
3. Memory mapping, 64K bytes in 128 byte blocks.
4. Real-time breakpoint.

1.4 TYPICAL APPLICATIONS

1. Monitor user program flow in real-time during prototype system development.

2. Perform product acceptance tests in production environment

3. Trouble shoot, field service faulty hardware logic, such as bad memory chips, I/O ports etc.

2.0 USER REQUIREMENTS

There are several SDOS commands with which the user should be familiar to fully utilize the HWA capabilities. The Hardware Analyzer supplement to the TWIN Operator's Guide explains the formats and the parameters of the individual commands. The following commands are available:

ICE - Turn ICE mode on/off

MAP - Map user or common memory

RTT - Arm Real-Time Trace

DRT - Dump Real-Time Trace

MOVE - Move a memory block to other location

READ - Read user memory, data or I/O port

WRITE- Write user memory, data or I/O port

2.1 A TYPICAL PROCEDURE

1. Turn ICE mode on.
2. Map memory to the user in the desired address range.
3. Move program code from common memory to user memory (if not already resident).
4. Arm Real-Time Trace.
5. Execute program.
6. Dump Real-Time Trace.

2.2 I/O CAPABILITY

The TWICE cable provides the necessary connection between the TWIN and the user's system.

2.3 USER PROBES

Pins 3, 4, 5, 6, 7 of the 16 pin socket (located on the upper right-hand corner of the PC board) provide the connection capability to user probes 0,1,2,3,4 and pin 2 to user probe 5, respectively.

Their displayed status follows the rules of "negative logic" (LOW=1)

3.0 PHYSICAL CHARACTERISTICS

Size:	11 x 7.4 inches (28 x 18.8 mm)
Weight:	12 oz.
Storage Temperature:	-55^{o} to $150^{o}C$
Operating Temperature:	0 to $70^{o}C$

3.1 POWER REQUIREMENTS

Voltage:	Current Typical	Current Maximum
+5V DC $\pm$ 5%	1.5 A	2.5 A
-12V DC $\pm$ 5%	3 mA	4 mA

4.0 REFERENCES

Signetics TWIN Operator's Guide

Signetics TWIN Real-Time Hardware Analyzer Supplement to Operator's Guide

Signetics TWIN Real-Time Hardware Analyzer Supplement to Maintenance Manual

Signetics TWIN 2650A/A-1 Slave CPU Supplement to Reference Manual

5.0 HARDWARE ORGANIZATION

The HWA consists of three basically independent functional blocks, although they share most of the buffer and control circuitry. The block diagram is shown in Figure 5.1.

5.1 REAL-TIME-TRACE

Real-time-trace logic, when enabled, captures up to 256 bus transactions of the Slave processor. The content of the trace memory can be stored and/or displayed on an output device.

5.2 SHADOW RAM

Shadow RAM is required to hold small programs for the Slave CPU that can not be placed in common memory because they could occupy a space that the user might want to use.

5.3 MEMORY MAP MEMORY

Memory map memory enables the user to assign any number of 128 byte blocks in the 64K slave memory address space, either to the TWIN common memory or to the user memory.

5.4 COMPATIBILITY

The HWA will be operational in any TWIN system when the 2650 Slave CPU board (**Part No. TW90012061JE**) is modified as follows:

A. Free pins 2 and 3 of IC B12 (7402)

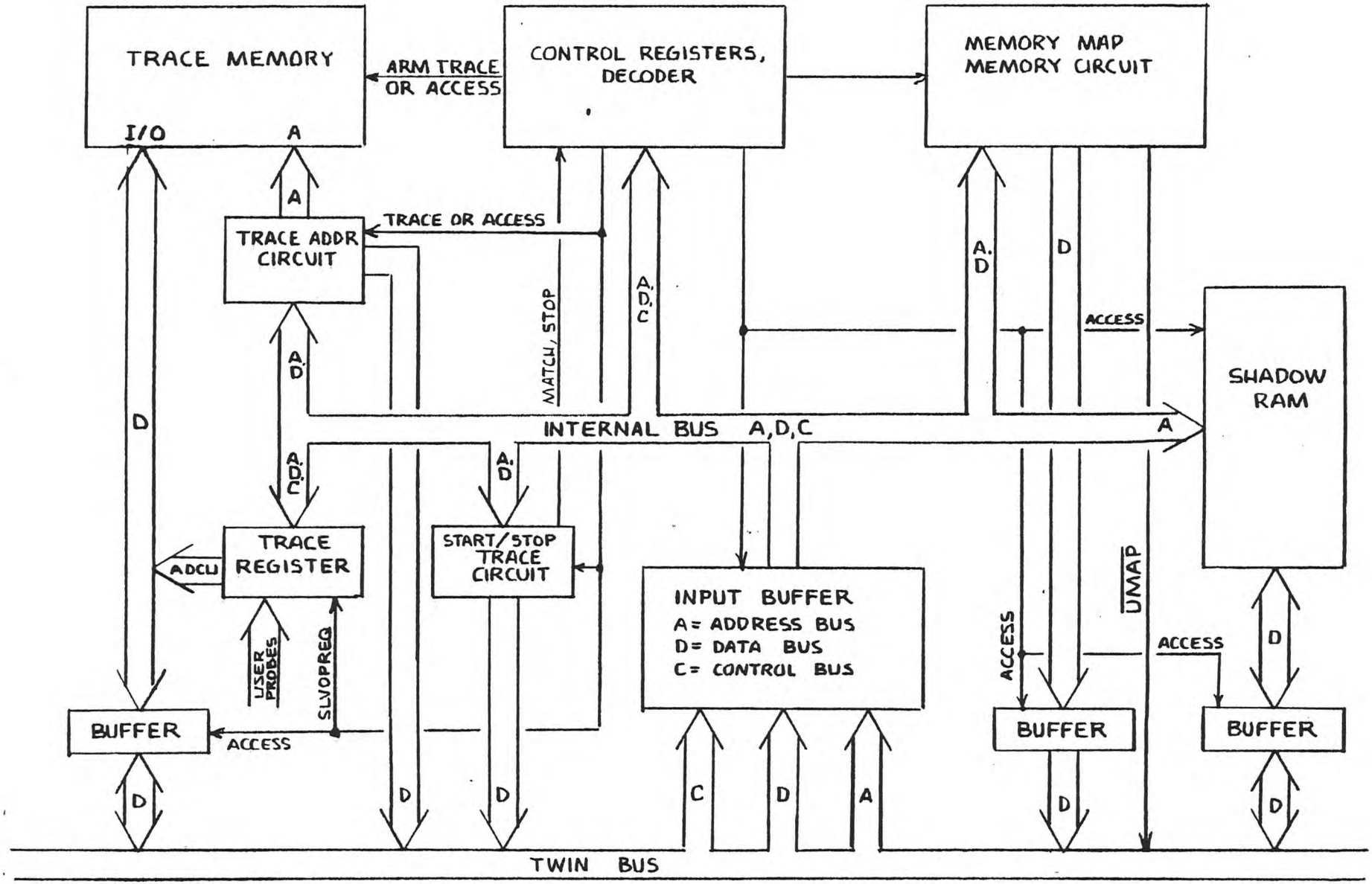
B. Connect IC B12 Pin 2 to IC B11 Pin 2

C. Connect IC B12 Pin 3 to edge connector P1-90.

D. Connect a 2.2K resistor between P1-90 and Vcc.

When using the 2650A/A-1 version of the Slave CPU board (Part No. TW90012061JE-A) the following jumpers changes must be made:

REMOVE	Jmpr.	1 - 2
REMOVE	Jmpr.	17 - 18
ADD	Jmpr.	2 - 3
ADD	Jmpr.	18 - 19



H.W.A FUNCTIONAL; BLOCK DIAGRAM

FIGURE 5.1

6.0 OPERATIONAL DESCRIPTION

The operating system (SDOS) initializes, reads the status of, or sets the new operating conditions of the HWA by setting it to "Access" mode. This is accomplished by sending a control byte with bit 0 = 1 to the HWA control port. In this mode, the Shadow RAM can be loaded, the memory map set, or the trace memory content displayed. If bit 0 of that control byte is 0, the HWA is in the "Trace" mode.

6.1 RTT

The Real-Time-Trace memory is organized as 4 blocks of 256 bytes each.

Operating Modes:

A. ACCESS MODE. The master CPU can access the trace memory as four consecutive blocks of 256 bytes, starting at address H'4000' in memory bank 1 of common memory. The bit and byte assignments are as follows.

ADDRESS	DATA	CONTENT
4000-40FF	B7-B0	A15-A8
4100-41FF	B7-B0	A7 - A0
4200-42FF	B7-B0	D7 - D0
4300-43FF	B7	FETCH
	B6	M/IO
	B5	R/W
	B4-B0	User 4 - 0 Probes

This mode is used mainly to read, interpret and display the trace memory contents by the operating system (DRT - Dump Real Time Trace command).

B. TRACE MODE. The Real-Time-Trace is armed by an RTT command. An armed trace enables the trace memory to be written as four parallel blocks of 256 bytes each on the trailing edge of the operation request ($\overline{\text{SLOPREQ}}$) signal from the Slave processor. The HWA can be programmed to capture the following types of transactions:

Instruction Fetches	(F)
I/O Access	(I)
Memory Access	(M)
Read Operatons	(R)
Write Operations	(W)
I/O Read	(IR)
I/O Write	(IW)
Memory Read	(MR)
Memory Write	(MW)
All Bus Transactions	(*)
Disarm Real Time Trace	(OFF)

The specified bus transactions are continuously stored in a cyclic manner until either the trace becomes disarmed or the slave processor is halted.

A 16-bit address comparator, in combination with a "trace stop counter" circuit, will stop the trace if an "address + count" (1-255) condition is specified and met. This feature enables the user to monitor up to 256 bus transactions before, after or around a valid address, depending on the value of the "count". In other words, "count" specifies how many more transactions will be stored after an address match has been detected.

A ground signal on User Probe 5 in conjunction with the slave processor running, will have the same effect as an address match; it arms the trace stop circuitry. This is used to monitor the bus transactions around a "trigger" signal.

6.2 SHADOW RAM

The Shadow RAM contains small SDOS routines that are executed by the Slave processor. NOTE: A system without the HWA holds the routines in the common memory where they could occupy a space the user might want to use. The Shadow RAM is loaded by the Master CPU during initialization. The Master accesses it at address H'44xx' during that operation. Whenever the Slave CPU executes the program, residing in Shadow RAM, it addresses it at H'54xx' or H'44xx', depending on the trace being armed or not, respectively.

6.3 MEMORY MAP

Memory map memory is a 512 bit map, where each bit represents a 128 byte segment of the 64K Slave memory space. Resetting or setting a bit through an SDOS command (MAP), the associated memory block is assigned to the user (external) or to the common memory (internal), respectively. The mapping algorithm always observes the 128 byte boundary; that is, it assigns the entire block to the appropriate system whenever a specific address falls within a boundary. The Master CPU accesses this memory at H'45xx'.

6.4 INTERFACE SPECIFICATIONS

All inputs ($\overline{ADR0}$ - $\overline{ADR15}$, $\overline{DATA0}$ - $\overline{DATA7}$, $\overline{OPREQ}$, $\overline{M}$/IO, R/$\overline{W}$, $\overline{WRP}$, $\overline{SLOPREQ}$, $\overline{RESET}$, $\overline{MASTRUN}$) represent one standard LS-TTL load for the system bus (I_{IL} = 0.4 mA, I_{IH} = 20 uA).

Output drives:

UMAP	I_{OL} = 20 mA, I_{OH} = -6.5 mA
RAMINH	I_{OL} = 40 mA, I_{OH} = -5.2 mA

7.0 CIRCUIT DESCRIPTION

7.1 INPUT BUFFER

Each incoming address, data and control signal is inverted to form a "HIGH=TRUE" internal bus.

7.2 CONTROL CIRCUIT (see Figure 7.1)

The Master CPU has access to the HWA control and status circuits through designated I/O ports by executing an EXTENDED READ or WRITE instruction. The assigned port addresses are from H'C0" to H'C5'. The READ/WRITE port decoder generates the proper control signal whenever a given port is addressed.

PORT ADDRESS	NAME/FUNCTION	ACCESS
C0	Control Byte	Write Only
C0	Status Byte	Read Only
C1	Trace Address Counter	Read/Write
C2	Trace Stop Counter	Read/Write
C3	Trace Address (high)	Read/Write
C4	Trace Address (low)	Read/Write
C5	Match Latch	Write Only

The main control circuitry is built around an FPLA. Figure 7.2 depicts the associated program table. The control byte register is set by the operating system when an RTT command is executed (address H'C0').

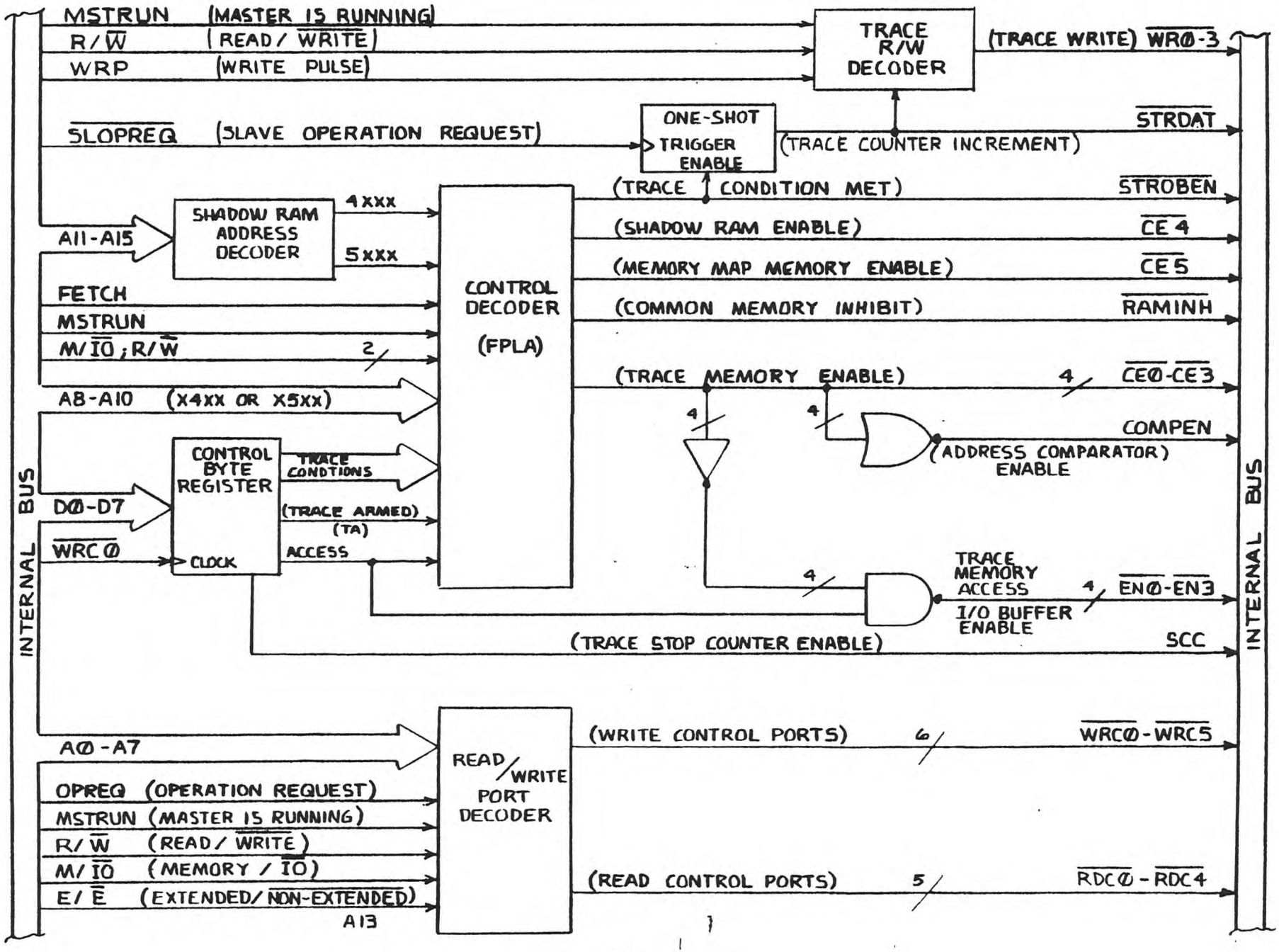

MSTRUN (MASTER IS RUNNING)
R/W (READ/WRITE)
WRP (WRITE PULSE)
SLOPREQ (SLAVE OPERATION REQUEST)
TRACE R/W DECODER
(TRACE WRITE) WR0-3
ONE-SHOT TRIGGER ENABLE
(TRACE COUNTER INCREMENT)
STRDAT
(TRACE CONDITION MET)
STROBEN
SHADOW RAM ADDRESS DECODER
A11-A15
4XXX
5XXX
(SHADOW RAM ENABLE)
CE4
(MEMORY MAP MEMORY ENABLE)
CE5
CONTROL DECODER (FPLA)
FETCH
MSTRUN
M/IO; R/W
(COMMON MEMORY INHIBIT)
RAMINH
(TRACE MEMORY ENABLE)
CE0-CE3
A8-A10 (X4XX OR X5XX)
COMPEN
(ADDRESS COMPARATOR ENABLE)
CONTROL BYTE REGISTER
TRACE CONDTIONS
D0-D7
(TRACE ARMED) (TA)
WRC0
CLOCK
ACCESS
TRACE MEMORY ACCESS
I/O BUFFER ENABLE
EN0-EN3
(TRACE STOP COUNTER ENABLE)
SCC
INTERNAL BUS
A0-A7
READ/WRITE PORT DECODER
(WRITE CONTROL PORTS)
WRC0-WRC5
OPREQ (OPERATION REQUEST)
MSTRUN (MASTER IS RUNNING)
R/W (READ/WRITE)
M/IO (MEMORY/IO)
E/E (EXTENDED/NON-EXTENDED)
A13
(READ CONTROL PORTS)
RDC0-RDC4

FIGURE 7.1

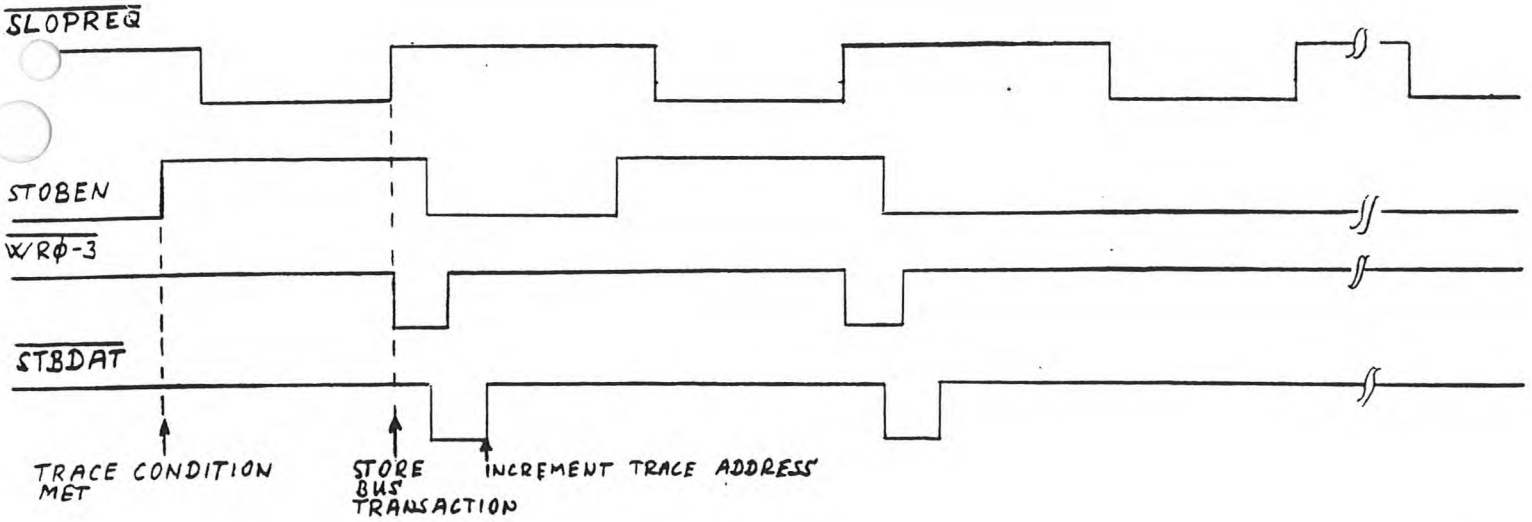


FIGURE 7.2a.

NO.	PRODUCT TERM* INPUT VARIABLE 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ACTIVE LEVEL H	L	L	L	L	L	L	H OUTPUT FUNCTION* 7	6	5	4	3	2	1	0
0	1		1	1		1	1		0	1	0													A							
1	1		1	1		0	0		0	1	0													A							
2	1		1	1				0	0	1	0													A							
3	1		0	0		1	1		0	1	0													A							
4	1		0	0		0	0		0	1	0													A							
5	1		0	0				0	0	1	0													A							
6	1				0	1	1		0	1	0													A							
7	1				0	0	0		0	1	0													A							
8	1				0			0	0	1	0													A							
9		0	1	1		1	1		0	1	0													A							
10		0	1	1		0	0		0	1	0													A							
11		0	1	1				0	0	1	0													A							
12		0	0	0		1	1		0	1	0													A							
13		0	0	0		0	0		0	1	0													A							
14		0	0	0				0	0	1	0													A							
15		0			0	1	1		0	1	0													A							
16		0			0	0	0		0	1	0													A							
17		0			0			0	0	1	0													A							
18									1		1		0	0	0	0														A	A
19									1		1		0	0	0	1							A								A
20									1		1		0	0	1	0						A									A
21									1		1		0	0	1	1					A										A
22			1						1		1		0	1	0	0				A											A
23			1						1		1		0	1	0	1			A												A
24									0	1	0										A	A	A	A							
25			1						1	0	0		0	1	0	0				A											A
26			1						1	1	0	0		1	0	0				A											A
27											0								A												
28																															
	FETCH	FETCH DON'T CARE (D3)	MEMORY/IO	MEM/IO POLARITY (D2)	M/IO DON'T CARE (D1)	READ/WRITE	R/W POLARITY (D7)	R/W DON'T CARE (D6)	ACCESS (D5)	TRACE ARMED (D4)	MASTER RUN	5XXX+OPREQ	4XXX+OPREQ	A11	A9	A8	STROBEN	CE5 (MEM. MAP)	CE4 (SHADOW RAM)	CE3 (F1,M/IO,4M,4)	CE2 (D7-D4)	CE1 (A7-A4)	CE0 (A5-A0)	RAMINH							

Figure 7.2

CONTROL BYTE BIT ASSIGNMENT

Bit 7 R/W Polarity

Bit 6 R/W Don't Care

Bit 5 M/IO Polarity

Bit 4 M/IO Don't Care

Bit 3 Fetch Don't Care

Bit 2 Arm Stop on Address Compare Plus Count

Bit 1 Trace Armed (when set)

Bit 0 Access Mode (when set)

When Bit 1 is set, the trace circuit becomes armed and the following output conditions will be present (see Figure 7.2).

A) If bit 0 (access) is not set and the Slave is running as well, all four blocks of the trace memory are enabled (term 24, $\overline{CE0\text{-}3}$ are low) and so is the address comparator (COMPEN = HIGH).

B) When the above conditions are true and any of the trace conditions are met (terms 0 - 17), the FPLA (STROBEN) enables a one shot circuit that will be triggered by the trailing edge of the Slave operation request signal. The resulting pulse (about 140 ns wide) STBDAT, in conjunction with the write pulse (WRP) and R/W signal from the Slave CPU, generates a write signal ($\overline{WR0\text{-}3}$) for the trace memory first, that causes the bus transactions to be stored, then increments the trace address counter. The timing diagram is shown in Figure 7.2a.

C) If bit 0 is set (access mode), the Slave is running and its address is at H'54xx' the shadow RAM enable ($\overline{CE4}$) and the common memory inhibit ($\overline{RAMINH}$) becomes true (term 26) so the Slave CPU can execute the programs stored in the shadow RAM. The same output conditions are present when the trace is not armed (bit 1 is 0) and the Slave

address is at H'44xx' (term 25). In other words, the Shadow RAM is accessed by the Slave CPU at H'44xx' when the trace is not armed and at H'54xx' when it is armed.

Whenever the Slave is running (term 27) or the Master CPU accesses (bit 0 = 1) address location H'45xx' (term 23), the memory map memory is enabled ($\overline{CE5}$ = low), plus in the last case, the common memory is inhibited ($\overline{RAMINH}$ = TRUE).

If the access bit is set (bit 0 = 1) and the Master is running, various memory types are enabled, depending on the address value presented by the CPU. The common memory is inhibited at the same time ($\overline{RAMINH}$ = LOW, terms 18 - 22).

ADDRESS	MEMORY TYPE	ACTIVE CHIP ENABLE
H'40xx'	Trace memory for A15 - A8	$\overline{CE0}$
H'41xx'	Trace memory for A7 - A0	$\overline{CE1}$
H'42xx'	Trace memory for D7 - D0	$\overline{CE2}$
H'43xx'	Trace memory for F, M/IO, R/W, User Probes	$\overline{CE3}$
H'44xx'	Shadow RAM	$\overline{CE4}$

The "chip enable" signals are gated with the "access" signals to form an enable for the trace memory input/output drivers.

7.3 SHADOW RAM (see Figure 7.3)

The shadow RAM is organized as 256 bytes of read/write memory, where 128 bytes are reserved for temporary data storage, the rest hold utility

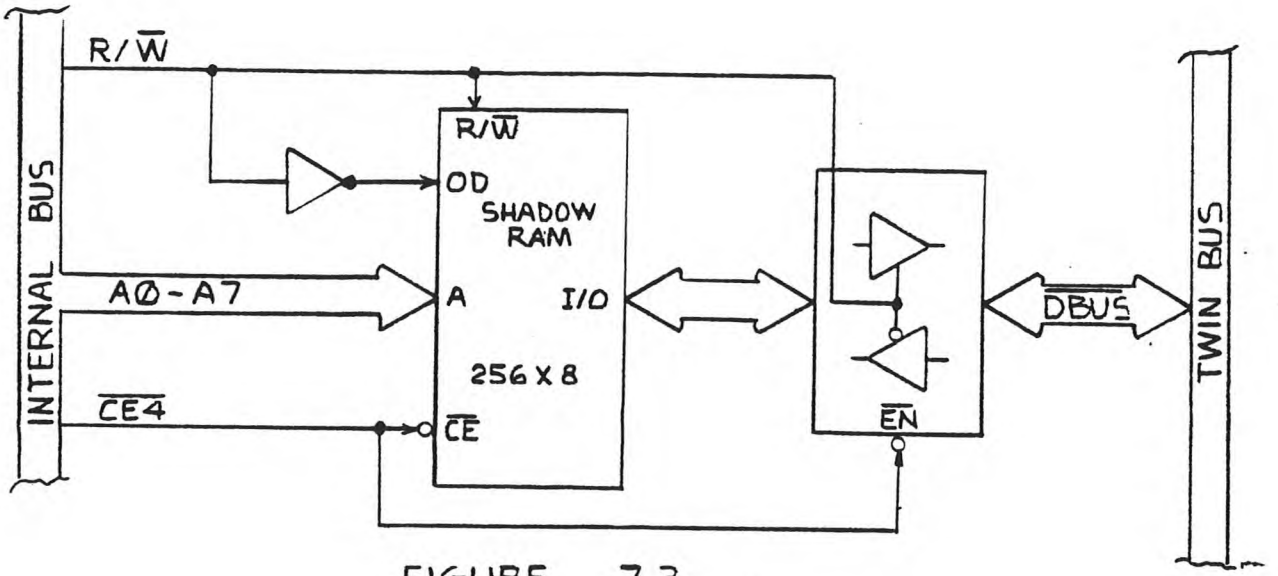


FIGURE 7.3

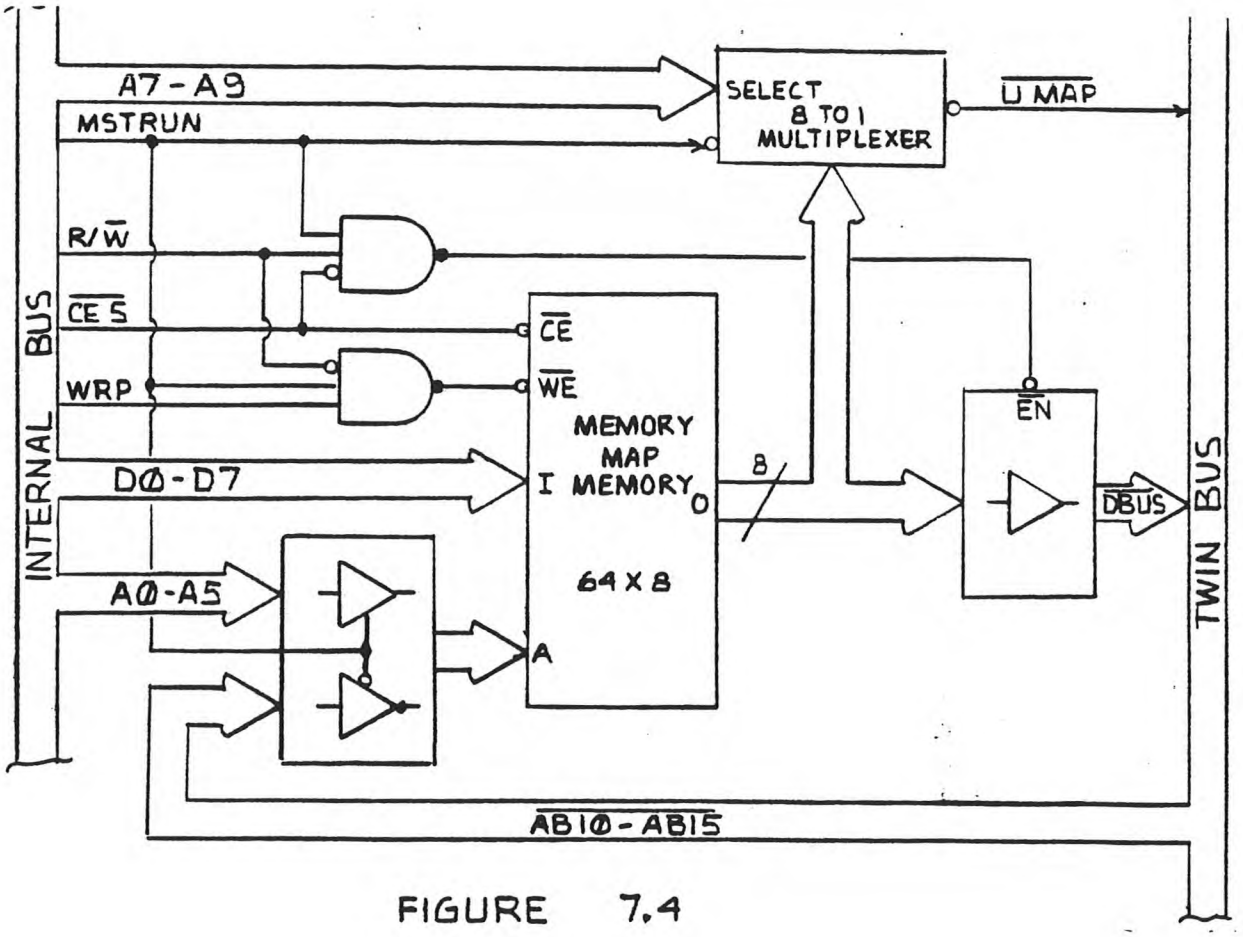


FIGURE 7.4

programs that are executed by the Slave CPU. The circuitry is enabled ($\overline{CE4}$ = LOW) under the following conditions (see terms 22, 25 and 26 of Figure 7.2). The operating system (SDOS) sets the access bit (bit 0 = 1) in the HWA control byte and:

A) Master CPU accesses memory at address H'44xx'. This happens mainly during system boot, where the shadow RAM is initialized.

B) The Slave CPU accesses memory either at address H'44xx', when the trace is <u>not</u> armed (bit 0 = 1 in HWA control byte), or at address H'54xx', when the trace <u>is</u> armed (bit 1 = 1). These conditions are satisfied when the SDOS memory handler is called or whenever the Slave CPU status has to be saved/restored for servicing an interrupt.

7.4 MEMORY MAP MEMORY (see Figure 7.4)

This circuit enables the user to assign an arbitrary number of 128 bytes of the 64K Slave CPU memory space to the user system, i.e., within specified address ranges, the Slave processor will fetch data from the external user memory (through the TWICE cable) and not from the internal, common memory, when the proper ICE mode (2 or ON) is selected. The UMAP circuitry is <u>always</u> enabled when the Slave CPU is running ($\overline{MASTRUN}$ = FALSE: $\overline{CE5}$ = TRUE in term 27 of Figure 7.2).

We mentioned earlier in paragraph 6.3, that the map memory contains 512 bits and each bit represents a 128 byte block in the 64K Slave address space. Here, we will describe how the actual mapping is accomplished.

The map memory is organized as a 64 x 8 read/write memory. Each byte, i.e., each address location of the map memory, will represent 1K byte (8

blocks of 128 bytes) of the Slave CPU address space. The six high order address lines (A10 - A15) of the Slave processor are routed to the map memory address inputs to select the corresponding byte for each 1K memory segment. The output data is decoded by an 8 line to 1 line multiplexer that, using the next high order address lines (A7 - A9), determines which 128 bytes block of that 1K is being addressed. If the corresponding bit is set, the multiplexer output (UMAP) becomes active to indicate that that particular address is mapped out to the user system.

The memory map memory is written or read by the operating system ($\overline{\text{MASTRUN}}$ = TRUE) at address location H'45xx' (see term 23 of Figure 7.2) whenever the access bit (bit 0) is set in the HWA control byte.

7.5 REAL TIME TRACE LOGIC (See Figure 7.5)

The Real-Time-Trace logic consists of three basic blocks:

A. Trace Memory Address Circuit

B. Trace Memory Circuit

C. Trace Stop Circuit

and operates in two modes: Trace or Access Mode.

The mode of operation is determined by the status of bit 0 (access) and bit 1 (trace armed) of the HWA control byte.

7.5.1 Trace Memory Address Circuit

In access mode (MASTRUN = TRUE, ACCESS = TRUE), the operating system has control over the trace memory by enabling one of the four RAM and I/O

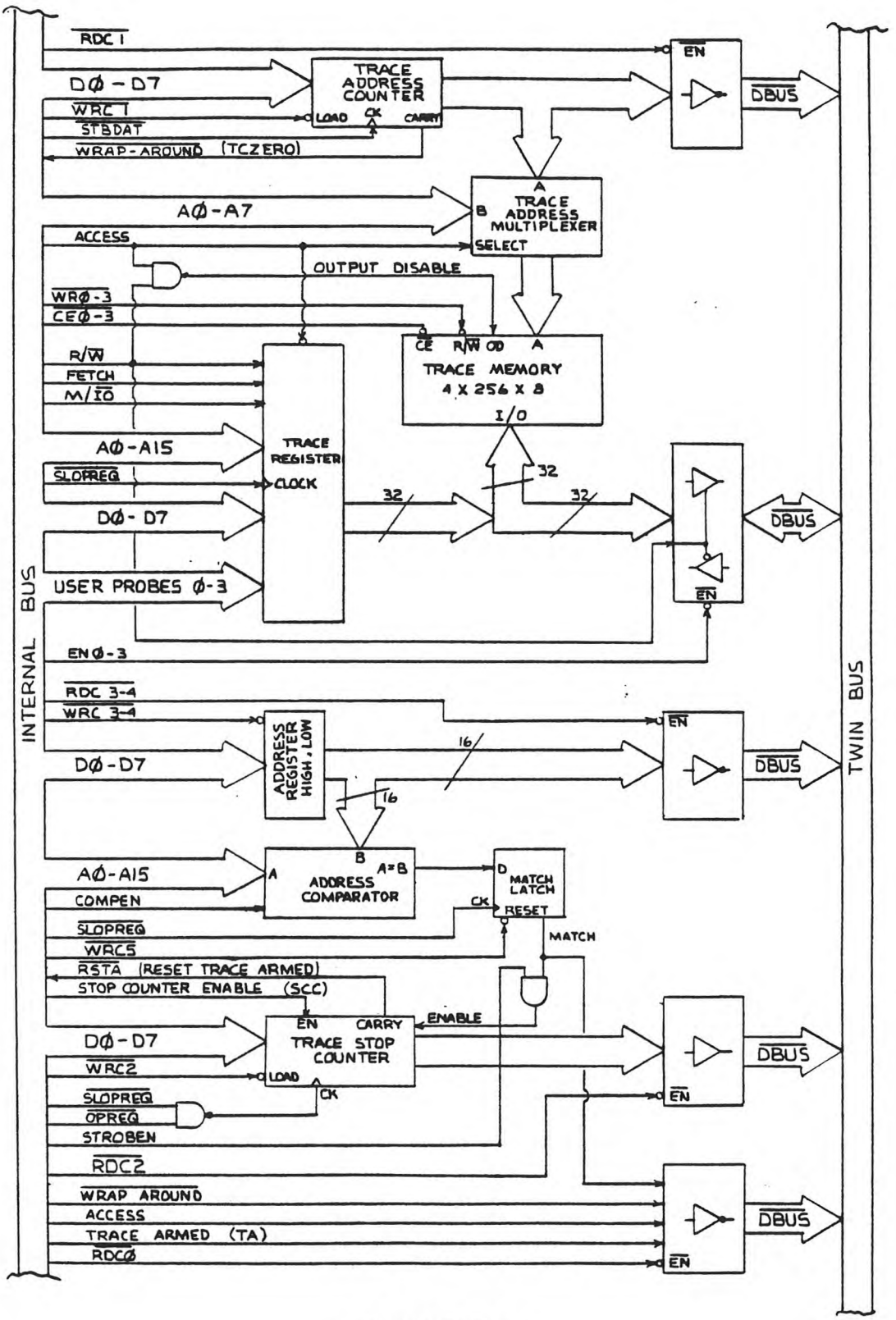

INTERNAL BUS
TWIN BUS
RDC 1
DØ - D7
WRC 1
STBDAT
WRAP-AROUND (TCZERO)
TRACE ADDRESS COUNTER
LOAD
CK
CARRY
EN
DBUS
AØ-A7
A
B
TRACE ADDRESS MULTIPLEXER
SELECT
ACCESS
OUTPUT DISABLE
WRØ-3
CEØ-3
R/W
FETCH
M/IO
CE
R/W
OD
A
TRACE MEMORY
4 X 256 X 8
I/O
AØ-A15
SLOPREQ
CLOCK
TRACE REGISTER
32
USER PROBES Ø-3
ENØ-3
RDC 3-4
WRC 3-4
ADDRESS REGISTER HIGH, LOW
16
B
A=B
A
ADDRESS COMPARATOR
COMPEN
SLOPREQ
WRC5
D
MATCH LATCH
RESET
MATCH
RSTA (RESET TRACE ARMED)
STOP COUNTER ENABLE (SCC)
ENABLE
EN
CARRY
TRACE STOP COUNTER
WRC2
OPREQ
STROBEN
RDC2
WRAP AROUND
ACCESS
TRACE ARMED (TA)
RDCØ

FIGURE 7.5

buffer blocks, depending on the address value (see terms 18 - 21 of Figure 7.2) that is between H'4000' and H'43FF'. The two most significant Hex digits are decoded by the FPLA providing the proper $\overline{CE}$ signal and the two least significant Hex digits address the 256 bytes of the trace memory through the Trace Address Multiplexer.

In trace mode (ACCESS = FALSE) an 8-bit counter is selected to address all four blocks of trace memory in parallel, which is incremented every time a STRDAT signal is generated by the control circuit. The Trace Address Counter can be pre-loaded by an Extended Write instruction to port H'C1' or its contents are read by executing an Extended Read to the same port ($\overline{WRC1}$ and $\overline{RDC1}$ signals). If more than 256 bus transactions have been traced, the counter generates a "wrap around flag" (TCZERO).

7.5.2 Trace Memory Circuit

The Trace Memory Circuit consists of four blocks of trace register, RAM and I/O buffer circuits.

In access mode, the trace registers are disabled and the RAM and I/O buffers enabled, as was described in paragraph 7.5.1.

In trace mode, (TRACE ARMED = TRUE) the trailing edge of the operation request signal from the Slave CPU ($\overline{SLOPREQ}$) loads the trace registers with the bus transactions (A0-A15, b0 - B7, FETCH, M/$\overline{IO}$, R/$\overline{W}$, User Probes). All four blocks of RAMS's are enabled in parallel input mode ($\overline{CE0}$ - $\overline{CE3}$ = TRUE, OD = TRUE), and the I/O buffers are tri-stated as well

($\overline{ENO}$ - $\overline{EN3}$ = FALSE). When a trace condition, specified by an RTT command, is met, the control circuit generates a write signal ($\overline{WRO - 3}$) for the RAMS's that load the trace memory with the trace register contents. (Right after that, the Trace Address Counter is incremented by $\overline{SRBDAT}$ - see paragraph 7.5.1). The above operation continues in a cyclic manner until the TRACE ARMED bit (bit 1) in the HWA control byte is reset to FALSE or until the Slave processor is halted.

7.5.3 Trace Stop Circuit

We have seen, in the previous paragraph, that the specified bus transactions are continuously stored in the trace memory (when TRACE ARMED = TRUE). The Trace Stop Circuit provides the means to reset the TRACE ARMED Bit (bit 1) in the HWA control byte at a specified address. This will make all input conditions in terms 0 - 17 of Figure 7.2 invalid, moving STROBEN to the inactive state, that inhibits the trace circuit ($\overline{STBDAT}$ and $\overline{WR\ 0 - 3}$ remain false).

The operating system sets a 16-bit address register to the desired value (specified by the RTT command) by an Extended Write operation to port H'C3' and H'C4' ($\overline{WRC3}$ and $\overline{WRC4}$). (It can read the contents of that register by reading the same ports - signals $\overline{RDC3}$ and $\overline{RDC4}$). This address value is continuously compared with the TWIN bus address in the trace mode (COMPEN = TRUE) and if a coincidence is detected, a latch is set to indicate the 'MATCH'. An 8-bit Trace Stop Counter will determine how many more specified transactions are going to be traced after the MATCH.

The Trace Stop Counter is pre-loaded by the operating system to a value of 0 through 255 (default = 128) according to the instruction in the RTT command. A MATCH enables the counter to be incremented whenever the specified trace condition is met (STROBEN = TRUE). When it reaches full count, its carry output ($\overline{\text{RSTA}}$ = TRUE) resets the TRACE ARMED bit in the HWA control byte; that is, stops the trace.

Writing or reading the Trace Stop Counter is accomplished by an Extended Write or Read instruction to port H'C2' ($\overline{\text{WRC2}}$ or $\overline{\text{RDC2}}$ signals), respectively.

7.6 STATUS BYTE

The HWA status is read by the operating system through port H'C0' (signal $\overline{\text{RDC0}}$).

8.0 TESTING REQUIREMENTS

The basic functionality of this product is tested by executing various SDOS commands.

8.1 I/O PORTS

Ten "Primitive Diagnostic Commands" are available to set or display the status of the I/O ports. The purpose and format of each command is described in a support document, titled HWA DIAGNOSTIC OVERLAY DESCRIPTION (see **Appendix** B). By setting each port to a known value when displaying its content, the proper state of each bit can be verified.

Example:

Command	Display
HWA T 00	--
HWA T	TRACE COUNTER = 00
HWA T FF	--
HWA T	TRACE COUNTER = FF

Any discrepancy between the entered and displayed data bits indicates a faulty signal path (hardware) for that port(s).

NOTE: The "Match Occurred" (3rd) or "Wraparound" (4th) bits of the status port will be reset (= 0) after executing a RTT or an HWA T HH command, respectively.

8.2 MEMORY MAP MEMORY

This part of the hardware is tested by executing MAP commands to set and display the memory map. Since each byte of the memory map memory represents 1K byte of slave memory it is a good practice to test it in 1K byte increments.

Example:

Command	Display
MAP C 0-FFFF	--
MAP	0000-FFFF = C
MAP U 0-3FF	--
MAP	0000-03FF = U (1st 1K bytes)
	0400-FFFF = C
MAP U 400-7FF	--
MAP	0000-07FF = U (1st & 2nd 1K bytes)
MAP	0800-FFFF = C
.	. .
.	. .
.	. .
.	. .
MAP U FC00-FFFF	--
MAP	0000-FFFF = U (all 64K bytes)

Unsuccessful mapping will point to faulty address or data lines in the memory map circuitry.

8.3 REAL-TIME-TRACE MEMORY

The trace memory circuitry is tested by tracing TWIN slave program. Any program is useful as long as if executes at least 256 specified trasactions and as long as the program flow is well defined and constant every time it is executed. The proper operation can then be verified by displaying the real-time-trace (DRT command) and comparing it with the known data flow.

Example:

1. Connect an INSTRUCTOR 50 unit through the TWICE cable to the TWIN system.

2. Map address range 17C0-1FFF (USE MONITOR program and buffer area) to the user:

   MAP U 17C0-1FFF command

3. Turn ICE mode ON:

   ICE ON command

4. Arm real-time-trace:

   RTT * 1800 255 command, where

   1800 is the starting address of the "USE MONITOR" program of the INSTRUCTOR 50.

5. Execute program:

   GO 1800 command

6. Display trace:

   DRT command

7. Compare trace with the program listing in the INSTRUCTION 50 users guide. A careful examination of differences will pinpoint the faulty signal path(s).

8.4 SHADOW RAM

This part of the hardware is verified by executing SDOS command(s) that use the SDOS memory handler (such as DUMP, MOVE, etc.)

8.5 DIAGNOSTIC AIDS

The entire memory space (H'4000-453F') is exercised by a Diagnostic Interface Program (DIP). All faulty address locations are displayed on the system console in the following format.

ADDRESS = XXXX WRITE = XX READ = XX

The DIP overlay writes a certain data pattern to each memory location then reads it back and verifies it. A mismatch causes the above message where the WRITE, READ labels show the data being sent and the data being received at that particular address location, respectively.

All other messages are self-explanatory.

Place a DIP diskette, that contains a D3All overlay in Drive 0 and boot it. When the prompt character ($) is displayed enter the command lines.

LO 3All (cr)

That automatically executes the diagnostic test and displays the faulty address locations, if any.

8.6 BURN-IN

The above test is continously executed by:

$SO 80 (cr)
$LO 3All (cr) commands

APPENDIX

APPENDIX A

PIN DESIGNATIONS

PIN	SIGNAL	DESCRIPTION
1-4	+5V	Logic Power Input
5-12	Not Used	
13-14	-12V	Power Input
15-16	Not Used	
17	$\overline{\text{ADR0}}$	Address Bit 0
18	$\overline{\text{ADR1}}$	Address Bit 1
19	$\overline{\text{ADR2}}$	Address Bit 2
20	$\overline{\text{ADR3}}$	Address Bit 3
21	$\overline{\text{ADR4}}$	Address Bit 4
22	$\overline{\text{ADR5}}$	Address Bit 5
23	$\overline{\text{ADR6}}$	Address Bit 6
24	$\overline{\text{ADR7}}$	Address Bit 7
25	$\overline{\text{ADR8}}$	Address Bit 8
26	$\overline{\text{ADR9}}$	Address Bit 9
27	$\overline{\text{ADR10}}$	Address Bit 10
28	$\overline{\text{ADR11}}$	Address Bit 11
29	$\overline{\text{ADR12}}$	Address Bit 12
30	$\overline{\text{ADR13}}$	Address Bit 13
31	$\overline{\text{ADR14}}$	Address Bit 14
32	$\overline{\text{ADR15}}$	Address Bit 15
33	Not Used	
34	$\overline{\text{RAMINH}}$	RAM Inhibit Output
35	Not Used	
36	$\overline{\text{DATA0}}$	Data Bit 0

PIN	SIGNAL	DESCRIPTION
37	$\overline{\text{DATA1}}$	Data Bit 1
38	$\overline{\text{DATA2}}$	Data Bit 2
39	$\overline{\text{DATA3}}$	Data Bit 3
40	$\overline{\text{DATA4}}$	Data Bit 4
41	$\overline{\text{DATA5}}$	Data Bit 5
42	$\overline{\text{DATA6}}$	Data Bit 6
43	$\overline{\text{DATA7}}$	Data Bit 7
44-51	Not Used	
52	$\overline{\text{M}}$/IO	Memory/IO Enable
53	$\overline{\text{WRP}}$	Write Pulse
54	$\overline{\text{OPREQ}}$	Operation Request (Master)
55	R/$\overline{\text{W}}$	Read/Write Command
56-58	Not Used	
59	$\overline{\text{RESET}}$	System Reset
60-74	Not Used	
75	$\overline{\text{SLVOPREQ}}$	Slave Operation Request
76-81	Not Used	
82	$\overline{\text{FETCH}}$	Fetch Operation
83	Not Used	
84	$\overline{\text{MASTRUN}}$	Master CPU Run Indication
85-89	Not Used	
90	$\overline{\text{UMAP}}$	User Memory Enable
91-96	Not Used	
97-100	GND	System Ground

APPENDIX B

HWA DIAGNOSTIC OVERLAY DESCRIPTION

Overview

The overlay does not interrupt with the HWA data base, shown in Figure 2, except in one case: When the HWA Control Byte is asked to be set or displayed.

A) HWA C HH writes HH to port HCPT (see Figure 9.3) and sets HWCNTL to HH.

B) HWA C displays the contents of HWCNTL to CONO, since input from the HCPT is actually HWA status.

In all other cases, set or display requests are WRTE and REDE through the appropriate I/O ports shown in Figure 9.3.

Command Summary

The HWA Command Summary is shown on the following page.

PRIMITIVE DIAGNOSTIC COMMANDS FOR THE HWA AND MEMORY HANDLER

HWA C
PRINT THE CURRENT HWA CONTROL BYTE

HWA C HH
SET THE HWA CONTROL BYTE TO HH

HWA S
PRINT THE HWA STATUS BYTE

HWA T
PRINT THE HWA TRACE COUNTER

HWA T HH
SET THE HWA TRACE-STOP COUNTER TO HH

HWA P
PRINT THE HWA TRACE-STOP COUNTER

HWA P HH
SET THE HWA TRACE-STOP COUNTER TO HH

HWA A
PRINT THE CURRENT TRACE-COMPARE ADDRESS

HWA A HHLL
SET THE TRACE-COMPARE ADDRESS TO HHLL

HWA
PRINT THE ENTIRE CURRENT HWA SCENARIO

```
*
*   HARDWARE ANALYZER I/O PORT EQUATES
*
HTCPT    EQU      H'C1'     HWA TRACE COUNT I/O PORT
HTSCPT   EQU      H'C2'     HWA TRACE-STOP COUNT I/O PORT
HISPT    EQU      H'C0'     HWA STATUS INPUT PORT
HCPT     EQU      H'C0'     HWA CONTROL BYTE OUTPUT PORT
HHPT     EQU      H'C3'     TRACE-STOP ADDRESS HIGH I/O PORT
HLPT     EQU      H'C4'     TRACE-STOP ADDRESS LOW I/O PORT
*
*   HARDWARE ANALYZER STATUS BYTE BITS  (HWSTAT)
*
HSWRP    EQU      H'08'     WRAPAROUND
HSMCH    EQU      H'04'     MATCH OCCURRED
HSARM    EQU      H'02'     ARMED RTT
HSACC    EQU      H'01'     ACCESS/TRACE MODE
*
*   HWA CONTROL BYTE BIT SETTINGS  (HWCNTL)
*
*
*   .... .1..   ARM "STOP ON ADDRESS-COMPARE PLUS COUNT"
*   .... ..1.   ARM "REAL-TIME TRACE"
*   .... ...1   ACCESS MODE (0=TRACE MODE)
*
OPCNT    EQU      H'04'     ARM "STOP ON ADDRESS-COMPARE PLUS COUNT"
OPARM    EQU      H'02'     ARM "REAL-TIME TRACE"
OPACC    EQU      H'01'     ACCESS MODE BIT
*
*   (QUALIFIERS)
*
*
*   .... 1...   FETCH
*   ...1 ....   MEMORY/ I/O
*   ..1. ....   MEMORY/ I/O POLARITY
*   .1.. ....   READ/WRITE
*   1... ....   READ/WRITE POLARITY
*
OPF      EQU      H'08'     F   INSTRUCTION FECTCHES ONLY
OPI      EQU      H'10'     I   I/O ACCESSES ONLY
OPM      EQU      H'30'     M   MEMORY ACCESSES ONLY
OPR      EQU      H'C0'     R   READ OPERATIONS ONLY
OPW      EQU      H'40'     W   WRITE OPERATIONS ONLY
OPIR     EQU      H'D0'     IR  I/O READS ONLY
OPIW     EQU      H'50'     IW  I/O WRITES ONLY
OPMR     EQU      H'F0'     MR  MEMORY READS ONLY
OPMW     EQU      H'70'     MW  MEMORY WRITES ONLY
OPALL    EQU      H'00'     *   ALL BUS TRANSACTIONS
*
*
```

HARDWARE ANALYZER DATA BASE EQUATES

```
*
*   POINTERS TO SDOS HARDWARE ANALYZER DATA BASE
*
HDBASE   EQU      H'24A3'   CRITICAL ORIGIN, NEVER CHANGES
*
TCNT1    ACON     HDBASE+0  INITIAL TRACE COUNTER
TCNT2    ACON     HDBASE+1  FINAL TRACE COUNTER
TSCNT1   ACON     HDBASE+2  INITIAL TRACE-STOP COUNTER
TSCNT2   ACON     HDBASE+3  FINAL TRACE-STOP COUNTER
HWSTAT   ACON     HDBASE+4  HWA STATUS BYTE
HWCNTL   ACON     HDBASE+5  HWA CONTROL BYTE
HWADDH   ACON     HDBASE+6  TRACE-STOP ADDRESS HIGH
HWADDL   ACON     HDBASE+7  TRACE-STOP ADDRESS LOW
HWRTFG   ACON     HDBASE+8  DATA BASE 'RESTORED' FROM FILE FLAG
SRHI     ACON     HDBASE+9  HIGH ADDRESS OF SHADOW RAM ROUTINES
SRBNK    ACON     HDBASE+10 SHADOW RAM BANK
HWAV     ACON     HDBASE+11 HWA AVAILABILITY (0=AVAILABLE, 1=NOT)
SMODE    ACON     HDBASE+12 SLAVE MODE
SRXEQ    ACON     HDBASE+13 HI SLV ADR FOR SHADOW RAM ROUTINES
CMEMH    ACON     HDBASE+14 HI ADDRESS OF COMMON MEMORY
CMEML    ACON     HDBASE+15 LO ADDRESS OF COMMON MEMORY
*
*
*
*   REAL-TIME TRACE MEMORY POINTERS (RTT BUFFER)
*   (IN ACCESS MODE, IS BANK 1 OF COMMON MEMORY)
*
AHIGH    ACON     H'4000'   HIGH ADDRESS
ALOW     ACON     H'4100'   LOW ADDRESS
ADATA    ACON     H'4200'   DATA BYTE
AMISC    ACON     H'4300'   TRANSACTION INFORMATION
*
*   DESCRIPTION OF 'AMISC' BITS
*
*   1... ....   FETCH
*   .1.. ....   MEMORY/ I/O
*   ..1. ....   READ/WRITE
*   ...1 1111   PROBES
*
*
```

POINTERS TO SDOS HARDWARE ANALYZER DATA BASE

REAL-TIME TRACE BUFFER DESCRIPTION

signetics

a subsidiary of **U.S. Philips Corporation**

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